IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 5, Issue 10, October 2017

ATPG Technique for Testing Circuits Using PRNG Algorithm

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Abstract: An Automatic test pattern generation technique using a pseudo-random number generator algorithm for testing combinational circuit is proposed. Rather than targeting a single fault pair at a time, the proposed System approach can distinguish multiple fault pairs in a single instance. For generation of automatic multiple non-repeating inputs which is used for testing the combinational circuit Pseudo-random generator can be used. New approaches are needed to reduce execution time and to improve fault coverage.

Keywords: PRNG-Pseudo-random number generator; ATPG; Algorithm; Testing; Fault distinguishing

I. INTRODUCTION

A common objective of testing is to detect all or most modeled faults. Fault diagnosis is the process of finding the fault candidates from the erroneous response. Any vector that can produce different responses for two different faults is called a distinguishing vector for those faults. Hence, to reduce the number of fault candidates, a test set that is able to distinguish between all distinguishable faults is highly desirable. Most test generation systems are built around core ATPG algorithm for

(1) Finding a test vector for a target fault

(2) Simulating faults to find how many have been detected by a given vector.

The system then attempts to find tests of high fault coverage because the primary objective is fault detection, i.e., presence or absence of faults. Basically, we generate tests that are redundant for fault detection and then hope that they will provide better diagnostic capability. To reduce the excess tests we may resort to optimization or removal of unnecessary tests. Conventional ADPG engines target single fault pairs at a time with Boolean values only. However, targeting single fault pairs may miss opportunities to find vectors that can simultaneously distinguish multiple pairs.

New approach include diagnostic test generation technique using a pseudo-random generator algorithm that can produce a compact diagnostic test set that can distinguish all the distinguishable fault pairs. such a formulation allows for efficient handling of multiple fault pairs, and each diagnostic test vector generated will be able to distinguish a large number of fault pairs at each iteration. Subsequently, smaller diagnostic test sets are generated. Deterministic test pattern generation algorithms are highly complex and time-consuming. New approaches are needed to reduce execution time and to improve fault coverage. An approach which provides the testing of the combinational circuit by providing multiple non-repeating test inputs in the text file format and the response of the circuit to those inputs will be available in the text file format. Comparison of the generated outputs with the standard required outputs leads to the fault identification in the combinational circuit.

II. PSEUDO-RANDOM NUMBER GENERATOR

A pseudorandom number generator (PRNG), also known as a deterministic random bit generator (DRBG) is an algorithm for generating a sequence of numbers that approximates the properties of random numbers.

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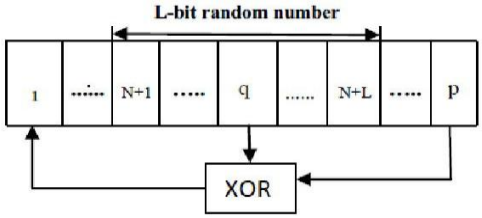

Fig.1 Random number generator using LFSR

The sequence is not truly random in that it is completely determined by a relatively small set of initial values, called the PRNG's state, which includes a truly random seed. pseudo-random numbers are important in practice for their speed in number generation and their reproducibility.

We use linear congruential method for generating random numbers which was introduced by D.H. Lehmer in 1949 which uses recurrence to generate numbers i.e.

Si = (a * Si-1 + c) mod m ------ (1)

Where, m = modulus

a = positive integer called the multiplier and c = positive integer called the increment

The Linear Congruential method has the advantage of being very fast, requiring only a few operations per call, hence it is almost used universally. The above recurrence (1) will eventually repeat itself, with a period that is obviously no greater than m. If m, a, and c are properly chosen, then the period will be of maximal length, *i.e.* of length m.

III. AUTOMATIC TEST PATTERN GENERATION METHODS

A) A Text I/O File based ATPG Technique
B) Diagnostic test generation Method
C) Modification in ATPG System
D) SMT-based Diagnostic Test Generation Method

A. A Text I/O File based ATPG Technique:

Conventional ADPG engines target single fault pairs at a time with Boolean values only. However, targeting single fault pairs may miss opportunities to find vectors that can simultaneously distinguish multiple pairs. The ability of random number generators to generate all the possible pairs of inputs will be utilized to generate inputs. Corresponding outputs will be noted. The noted outputs will be compared with the actual expected outputs for given input combination.

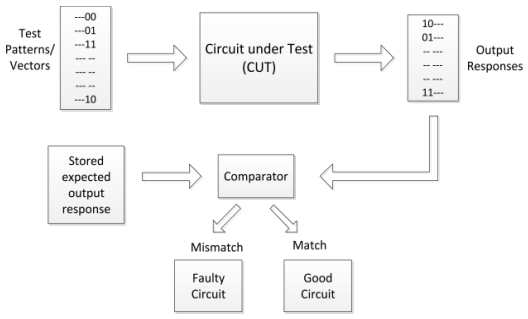

Fig.2 Proposed Methodology

An approach is a new diagnostic test generation technique using Pseudo-random number generator which is the algorithm that can automatically produce long runs of number with good random properties that can produce a compact diagnostic test set that can distinguish all the fault pairs. For generation of automatic multiple non repeating inputs which are used for testing the combinational circuits, pseudo-random generator can be used. Such a formulation allows

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for efficient handling of multiple fault pairs, and each diagnostic test vector generated will be able to distinguish a large number of fault pairs at each iteration. The VLSI combinational circuit is developed by writing it in either the VHDL language. The program so written is checked for errors, if any, in the **Quartus II 9.1 SP2**.The RTL view is developed by writing it in either the VHDL language.

IV. COMPUTATIONAL ANALYSIS

We use Lehmer linear congruential algorithm for the generation of random numbers which is called as test inputs

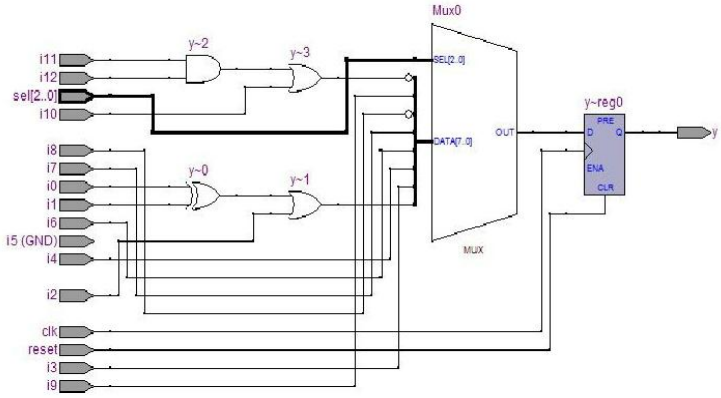

Fig.3 RTL View of Normal Circuit

We take 8:1 multiplexer which have 8 inputs, 3 select lines,5 combinational inputs means total 16 inputs can be applied which gives 2m = 65536, different input pair of combinations. We develop VHDL coding in structural modeling style for the normal circuit and get the related outputs of that circuit.After compilation on Quartus II software, we get RTL view of normal circuit. We can see the output waveform on modelsim software. Our approach is to test the combinational circuit which is taken into consideration whether it was faulty or not. If the circuit was faulty then we correct logic behind coding of lehmer algorithm.

We have one normal circuit with their inputs and outputs. We use different combinational gates in the normal circuit which is used for testing. We can added fault in some inputs of gates like (io xor i1), (i2 and i2), (not i3). Then get the outputs of faulty

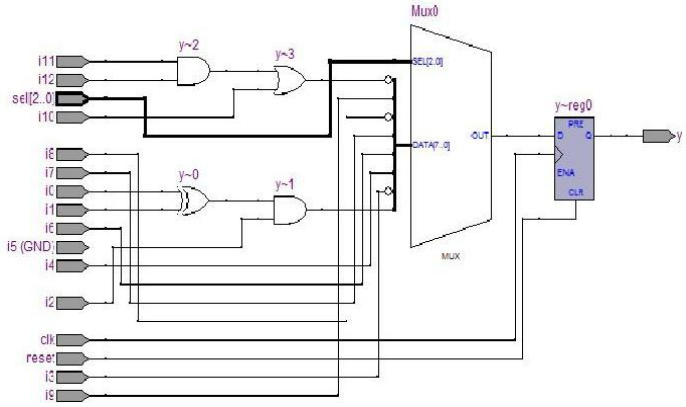

Fig 4 RTL View of Faulty Circuit

circuit. After compiling on Quartus II software we get RTL view of faulty circuit. We compare the output of normal circuit output with faulty circuit output which leads to fault identification. Output waveform of faulty circuit can be seen on modelsim software. Different gates like xor gate, And gate, Not gate, Ex-or gate for the different combination of the circuit. Quartus II software will be used for the compilation of the proposed VLSI design program written in VHDL or Verilog language of VLSI design programming. The errors if any will be detected by this software. This software also generates the RTL view of the proposed CUT which can give the better idea about the circuit.

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V. COMPARISON OF EXPERIMENTAL AND COMPUTATIONAL RESULT

Table I. Comparison of Parameter of Lehmer and Galois Algorithm

Algorithms	Power Dissipation	Time of Clock	Total Logic Element
Lehmer Congruential Method	21.28mw	9.746ns	16/18.75
LFSR Method by Galois	21.50mw	9.789ns	27/18.75

VI.CONCLUSIONS

The proposed work will give an Automatic Test Pattern generation (ATPG) method of fault testing in VLSI design by utilizing the concept of Pseudo-Random number Generators algorithm. This method ensures the less testing time, low testing cost, exact diagnosis of fault, an accurate diagnosis report available in text format. It requires less power consumption and improve testing efficiency. It avoid over-testing and manages under-testing.

ACKNOWLEDGMENT

I express my sincere gratitude to **Dr. R. M. Rewatkar**, Associate Professor at DMIETR, Wardha and **to Dr. Y. B. Gandoole**, Associate Professor at Adarsh Mahavidyalay,Dhamangaon Railway for extending his valuable insight for completion of this work.

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BIOGRAPHIES

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